DETECTING THE STATUS OF AN ELECTRICAL FUSE

FIELD OF THE INVENTION

[0001] The invention relates to detecting the status of an electrical fuse, and, more particularly, to a method and electrical circuit for testing the status of an electrical fuse in a semiconductor circuit.

BACKGROUND

[0002] US 6,384,664 discloses a fuse circuit for detecting the resistor difference between a poly fuse under detection and a matching reference fuse, which are in two legs at a top of an electrical bridge circuit. Two more legs at a bottom of the electrical bridge circuit have matched transistors. When the fuse under detection is not burned, the differential voltage across the bridge circuit remains at zero. When the fuse is burned, a comparator detects a transition in differential voltage across the bridge circuit. The comparator has a flip flop latch that will trip and store the data. The differential voltage is impressed on an output of an inverter with a long decay pulse, which delays turn off of the differential voltage before the latch trips. Because of difficulty to predict the slope of the inverter decay voltage, the timing of the latch trip lacks control. No control logic exists that would control the timing. The fuse circuit is unable to adjust its sensitivity to detect the fuse resistance value.

[0003] US 6,498,526 discloses a fuse circuit for detecting the resistor difference between a fuse under detection and a reference fuse, which are in an electrical bridge circuit that produces a differential output current proportional to the resistor difference. The system logic of an EPROM has an MRS1 register that provides a control signal pulse. A second MRS2 register of the EPROM provides a fuse program signal pulse. The fuse under detection can be programmed with a resistance value. The status of the value is indicated by the value of the differential output current. A disadvantage is that the control signals MRS1 and MRS2 operate by precisely timed steps; precharge, generate a voltage and place on a sensing circuit, and latch the detected value data. Such timing is difficult to control due to process variations that fabricate manufactured variations in semiconductor structures. A further disadvantage is that the fuse status value data is shifted to a register of the EPROM system logic. Manufactured variations in semiconductor

structures alter the timing by the control signals MRS1 and MRS2, which causes rippling and corruption of the status values, while being shifted to a register as retained data.

SUMMARY OF THE INVENTION

[0004] The invention is a fuse detection circuit having a latch sensing circuit and a timing control circuit that turns off the fuse detection circuit independently of a read signal decay. The sensing circuit has an adjustable sensitivity for detecting the fuse resistance value of a programmable poly fuse. The circuit is self timing by control logic to prevent data rippling and corruption. The status value data of the fuse is stored in the sensing circuit, which eliminates the need to shift the data to an external register.

[0005] A further advantage of the invention, is that a poly fuse under detection is in a bridge circuit that is adjustable in sensitivity to the fuse status data, to avoid confusion by slight variations in either programming or burning the fuse.

[0006] An embodiment of the invention will now be described by way of example with reference to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] FIG. 1 is a diagram of a fuse detection circuit according to the invention.

[0008] FIG. 2 is a diagram of a detection circuit.

[0009] FIG. 3 is a timing diagram.

DETAILED DESCRIPTION

[0010] Terms concerning attachments, coupling and the like, such as "connected" and "interconnected," refer to a relationship wherein structures are secured or attached to one another either directly or indirectly through intervening structures, as well as both movable or rigid attachments or relationships, unless expressly described otherwise.

[0011] Fig. 1 discloses a fuse bridge circuit (100) having a fuse resistance $R_{\_fuse}$, of a poly fuse (102) under detection, connected between a first reference voltage V1 and a first node (104). An MN6 transistor (106), for example, an NMOS transistor, has its drain connected to the first node (104), and its source connected to a second reference voltage V2, for example, ground, also referred to as, earth.

[0012] Fig. 1 further discloses fuse resistance $R_{\_ref}$, of a reference poly fuse (108) connected between the first reference voltage V1 and a second node (110). An MN5 transistor (112), for example, an NMOS transistor, has its drain connected to the second node (110), and its source connected to the second reference voltage V2.

[0013] The w/l ratio, the width to the length ratio of the MN6 transistor is four times that of the MN5 transistor. Thus, the ratio of current of MN5 transistor to current of MN6 transistor is 1:n, where n=4 .This ratio can be tuned to adjust the sensitivity of the sensing circuit.

[0014] The gates of MN5 and MN6 are connected to produce ΔV across the fuse bridge circuit.

[0015] $\Delta V = (I)(R_{\_fuse}) - (I)(4)(R_{\_ref})$

[0016] When $R_{\_fuse} < 4(R_{\_ref})$, then $\Delta V < 0$.

[0017] When $R_{\_fuse} > 4(R_{\_ref})$, then ΔV, >0.

[0018] Before the $R_{\_fuse}$ is burned, the resistances $R_{\_fuse}$ and $R_{\_ref}$ are equal, and $\Delta V<0$. After the fuse $R_{\_fuse}$ is burned, the resistance $R_{\_fuse}$ is greater than $4(R_{\_ref})$, and $\Delta V>0$.

[0019] Thus, by adjusting the current source ratio from 1:n, the blown fuse will be recognized when the blown poly fuse resistance value is greater than $(n)(R_{\_ref})$. The sensitivity of detecting the $R_{\_fuse}$ resistance value variation is increased.

[0020] Fig. 2 discloses a detection circuit having the fuse bridge circuit (100) of Fig. 1. An MP3 transistor (113), for example, a PMOS transistor, has its source connected to node (110) and its drain connected to a Vout node (114), and passing a reference voltage at voltage Vout. Similarly, an MP4 transistor (116), for example, a PMOS transistor, has its source connected to node (104) and its drain connected to a VoutB node (118) and passing an output voltage at voltage VoutB.

[0021] An input read signal pulse from an external source at read input terminal (120) is first supplied to an inverter (122) that produces an inverted read signal pulse ensa. The drains of MP3 and MP4 are connected together and to the output side of the inverter (122) to receive the read signal pulse ensa, which turns on the fuse bridge (100) and generates the voltage difference between voltages Vout and VoutB at respective nodes (114) and (118). During the pulse period when the read signal is inverted high, MP3 and MP4 will pass the voltage difference VoutB-Vout to the sensing circuit having MN1 and MN2 transistors (126) and (128), for example,

NMOS transistors. This voltage difference VoutB- Vout will have the same duration as the read signal pulse. This voltage difference between Vout and VoutB is sensed in a sensing circuit (124) after the read signal goes low.

[0022] The inverted read signal pulse ensa turns on MN3 transistor (130), for example, an NMOS transistor, with its source connected to ground, and its drain connected to the sources of MN1 and MN2 transistors (126) and (128). MN1 transistor (126) has its gate connected to Vout node (114) and its drain connected to node VoutB node (118). MN2 transistor (128) has its drain connected to Vout node (114) and its gate connected to VoutB node (118).

[0023] The read signal pulse decay or transition activates a latch circuit (136) having the MP1 transistor (132) and MP2 transistor (134) and the MN1 transistor (126) and the MN2 transistor (128), forming the complementary latch circuit (136). When the read signal pulse ensa decay or transitions, the MN3 transistor (130) turns off, which turns off the MN1 and MN2 transistors (126) and (128), and which turns on the MP1 and MP2 transistors (132) and (134), which pass the status value of VoutB-Vout = ΔV . When the $R_{\_fuse}$ is not burned, $\Delta V < 0$. When the $R_{\_fuse}$ has been burned its resistance is greatly increased in the fuse bridge circuit (100), and $\Delta V > 0$.

[0024] Fig. 2 further discloses a timing control circuit (138). The two current pulse inputs of XNA1, NAND gate (140), connect to the Vout and VoutB nodes (114) and (118) and produces an output signal during the coincident durations of the Vout and V outB pulses. The output signal of XNA1 and the inverted read signal pulse ensa are supplied as two current pulse inputs of a XNA2 second NAND gate (142) of the timing control circuit (138). The output of the XNA2, NAND gate (142), allows the conduction of the fuse bridge current enfb to continue until the XNA2, NAND gate (142), ceases to be conductive.

[0025] Fig 3. discloses a timing diagram. The input read signal pulse (300) is inverted by the XIN1 inverter (122) to provide the inverted ensa read signal pulse (302) of substantially the same duration as the read signal pulse (300). The enfb fuse bridge current (304) and the voltage difference between Vout (306) and VoutB (308) are activated by the ensa read signal pulse (302). The $R_{\_fuse}$ status data, is sensed by the sensing circuit (124), and the data is latched by the latch circuit (136) that is enabled, i.e. activated, by the decay or transition of the ensa read signal

pulse. After latching the fuse data in Vout (136), the timing control circuit (138) then will turn off the fuse bridge current, whereby enfb goes low.

[0026] The timing control circuit (138) is the control logic to turn off the fuse bridge current, which turns off the voltages VoutB and Vout. Because the timing control circuit (138) is in a feedback circuit with the fuse bridge circuit (100), it turns off the fuse bridge current, only after the fuse data has been sensed, and stored locally in the sensing circuit (124). The timing control circuit (138) is not turned off until the enfb fuse bridge circuit (304) has been turned off. Premature turn off of the enfb fuse bridge current is avoided. Because the timing control circuit (138) is in the feedback circuit, the turn off of the fuse bridge current by the timing control circuit (138) is independent of the read signal decay or transition.

[0027] Fig. 3 further discloses that the enfb fuse bridge current has a turn off that is delayed by the timing circuit (138), allowing time for latching of the status value data. The decay or transition of the Vout is the key value that switches XNA1 to a non-output state to shut of the enfb fuse bridge current after the activation of the latch circuit (136).

[0028] A further advantage of the invention, is that the status value data of the fuse (102) under detection is stored in the sensing circuit (124), which eliminates the need to shift the data to an external register.

[0029] A further advantage of the invention, is that the circuit (100) is self timing by control logic to prevent data rippling and corruption.

[0030] A further advantage of the invention, is that the bridge circuit (100) is adjustable in sensitivity to the $R_{\_fuse}$ status data, VoutB- Vout = ΔV, to avoid data confusion by slight variations in either programming or burning of the fuse (102).

[0031] Although the invention has been described in terms of exemplary embodiments, it is not limited thereto. Rather, the appended claims should be construed broadly, to include other variants and embodiments of the invention, which may be made by those skilled in the art without departing from the scope and range of equivalents of the invention.

[0032]